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A Switched Capacitor Boost Multilevel Inverter with Reduced Switches and Voltage Stresses

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ABSTRACT
The paper introduces a five-level double-boost switched capacitor inverter configuration which is useful for the application of (PV) systems. The basic construction of the circuit consists of six IGBT switches, one diode, a single capacitor, and a DC supply to produce five levels of the inverter's voltage with double boosting capability. Without the use of an auxiliary circuit or complicated algorithms, the used capacitor considers being a self-balanced voltage. The description, mathematical analysis, and operation modes of the circuit are described. A modulation strategy and a simple control technique are applied. The performance features of this proposed circuit are demonstrated by using (MATLAB-Simulink) software. A prototype for (SCDBMLI) is carried on and tested in the lab to validate the inverter. The outcomes from simulation and experiment have been examined in a variety of conditions. Additionally, the proposed topology has been confirmed by great agreement between the experimental and simulation results.

Keywords*: Boost Multilevel Inverter; Switched Capacitor; Modulation Index.*

1. INTRODUCTION

The deterioration of traditional resources has increased interest in renewable energy. Certainly, one of the most significant sources of renewable energy is the photovoltaic (PV) system since it operates without generating any noise or pollution and requires little maintenance. Thus, we need to improve appropriate power converters to extract high power quality from photovoltaic systems. Grid-connected PV systems generally contain photovoltaic modules and a power conversion step. The power conversion step includes for conversion two steps: first step; DC/DC converter and second step; DC/AC inverter. In DC/AC inverter, to produce an AC waveform, traditional inverters are employed, which need bulk filters on the output terminal to decrease the harmonics. Previous topologies have a modified configurations to replace traditional inverters with multilevel inverters (MLI) [1, 2].

The multilevel inverter generates a staircase waveform, which improves the harmonics and reduces voltage stress on switches [3]. Low voltage rating switches can be used in multi-level topologies in place of a high voltage switches as in the conventional inverters. Low voltage rating switches are typically smaller, less expensive, and capable of handling higher switching frequencies. Consequently, conduction losses are decreased as a result of a lower forward voltage drop. Moreover, losses across switches are reduced due to a lower dv/dt. [4].

Additionally, when the number level rises, the output signal's power quality and total harmonic distortion (THD) are both enhanced. The output filter size may be decreased as a result [5]. The three most common public types of multilevel inverters are the diode/clamped (NPC) [6], capacitor/clamped (FC) [7], and cascaded H-Bridge (CHB) [8]. For the generation of multilevel voltage, diode-clamped and capacitor-clamped multilevel inverters require a significant number of flying capacitors and clamped diodes. Cascaded H-bridge topologies can mitigate these drawbacks, which have some limitations of their own, such as the need for a separate dc source for each H-bridge [9].

These topologies don't have the capability of boosting. Some changes to the traditional cascaded multilevel inverter (CMLI) are possible. To get the load voltage in boost CMLI (BCMLI), a boost chopper is located among the input supply and H-bridges in place of magnetic components like transformers [10-12]. The increasing quantity of switches and DC supply reduces the efficiency and ability to handle of the CMLI and BCMLI topologies. Thus, certain adjustments may be

made using conventional CMLI and BCMLI systems. A boost chopper is integrated between the input supply and the DC-link inverter in a system called boost DC-link (CMLI), also known as BDCLCMLI [13]. The boost chopper system aims to raise DC voltage levels. The number of DC supply and power switches in this architecture is already minimal, albeit not noticeably so. As a result, additional power semiconductors and associated driving circuits are required as the levels rise. High system cost and complexity take essential factors into consideration. The article [14] suggests "reduced circuit number" and "maximizing the output level" due to the aforementioned restriction of classical MLIs. This structure, however, is unable to raise the input voltage.

These limitations are often overshadowed by another new approach called "switched-capacitor topology" for reducing the need for many elements and increasing the input voltage; additionally, multiple DC supplies are alternated by capacitors, which reduce cost and size; however, the limitations can be mitigated by using the switched capacitor approach, which reduces the need for numerous components while also boosting the input voltage, resulting in multiple [15]. So, the merits of using a Switched-Capacitor Boost Multilevel Inverter:

- It reduces DC sources count, lowering the cost and volume.
- The total stand voltage (TSV), power loss, and overall efficiency are all reduced while the device's number is decreased.
- It increases voltage without adding more inductors and transformers.
- It requires fewer components to provide the output voltage.

The topologies presented in [16-21] have the same boosting factor value and a higher count of components, which makes the system bulkier, costlier, and more complex. Furthermore, the topology of [22] presents a switched capacitor-based five-level MLI with lower components than the previous topologies, but the boosting feature is also missing. So, this paper lacks the main benefit of using switched capacitor technique which is the boosting of input dc supply. A single-stage five-level topology has been presented in [23] and [24]. These topologies are used for five levels across the load with a double voltage gain, and it has the same count of switches as the proposed configuration. But it has more capacitors than the suggested configuration. The suggested configuration has a lower $TSV_{p.u.}$ value than topologies [16, 17], [19-22] and [24]. However, in topology [23] has a lower $TSV_{p.u.}$ than the proposed topology but it has more components like the number of capacitors and diodes, which adds more weight, additional cost, and complexity to the circuit than the proposed topology. This paper describes a 5-level switched capacitor boost inverter with double voltage boosting at the output terminal by using a fewer count of devices. The total stand voltage (TSV) of the switches considers being low. There is no need of using a supplementary circuit to balance voltage across capacitor voltage.

The paper outlines are displayed as follows: The different operation modes for the suggested inverter are discussed in part (2). Part (3) and part (4) highlight the switching strategy for the circuit and the balance of the voltage capacitor, respectively. Part (5) is a comparative study between the suggested configuration and other similar topologies. Part (6) outlines the losses calculations for the proposed configuration. Part (7) examines the simulation and experimental outcomes under several circumstances. Finally, in part (8) concluded the article.

2. PROPOSED BOOST MULTILEVEL INVERTER

2.1 Architecture of the suggested configuration

The suggested boost multilevel inverter is illustrated in figure 1. The circuit produces a five-level output waveform with boosting capability in which the inverter's voltage is equivalent to twice the supply voltage. The proposed circuit consists of only six semiconductor devices, one diode, and a single capacitor also with a DC supply. According to the switches' states, which are listed in table 1, the proposed inverter has five operational modes, which are depicted in figure 2.

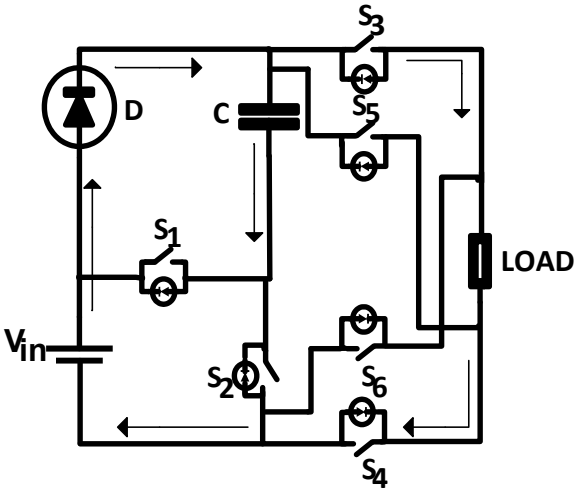


Figure 1. Proposed Circuit

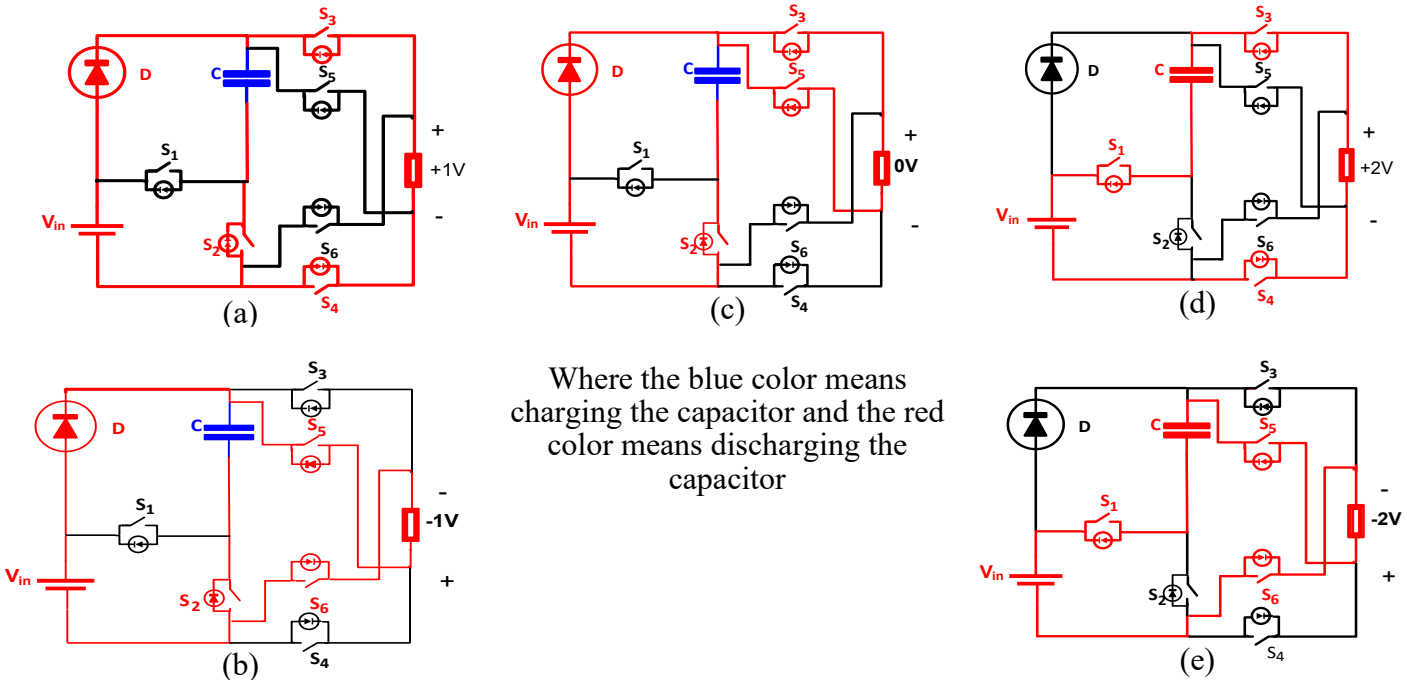


Figure 2. Switching states for the proposed scheme during operation modes

2.2 :Operation modes

2.2.1 Mode A, and B (± 1 level): (figure 2(a) and figure 2(b)) show mode A and mode B, respectively. In mode (A), the inverter's output is ($+V_{in}$) via switches (S_3 and S_4). In mode (B) (Figure 2(b)) the inverter's output is ($-V_{in}$) via switches (S_5 and S_6). Capacitor (C) is charging up to V_{in} through (D and S_2) during two modes

2.2.2. Mode C (0 levels): In mode (C) (figure 2(c)), the inverter produces a zero voltage by using (S_3 and S_5) and the DC supply charged capacitor (C) through (D and S_2)

2.2.3. Mode D and E (± 2 levels): (figure 2(d) and figure 2(e)) show mode D and mode E, respectively. In mode (D), the inverter's output is ($+2V_{in}$) by using switches (S_1, S_3, S_4). In mode (E), the inverter's output is ($-2V_{in}$) using switches (S_1, S_5, S_6). The DC source in series with Capacitor (C) is connected to the load to produce double voltage at the output terminal.

Table 1 shows a switching pattern in which 1's mentions to the (ON) state and 0's mentions to the (OFF) state for switches. And thestate of the capacitor **(↑)** means charging, while **(↓)** means discharging.
Table [2] provides an illustration of the voltage stress on components. Different voltage stresses are present in the switching devices; S_1 and S_2 are affected by voltage stresses equal to the input voltage.

Table 1. Capacitor state and switching states for circuit

mode	State of switches						State of capacitor	o/p voltage level
	S_1	S_2	S_3	S_4	S_5	S_6		
A	0	1	1	1	0	0	↑	1+
B	0	1	0	0	1	1	↑	1-
C	0	1	1	0	1	0	↑	0
D	1	0	1	1	0	0	↓	2+
E	1	0	0	0	1	1	↓	2-

However, voltage stresses on switches (S_3, S_4, S_5, and S_6) are equivalent to the inverter's output voltage. Equation (1) is used to determine total standing voltage (TSV):

$$TSV = \frac{\sum_{i=1}^{n} V_{bswitch,i} + \sum_{j=1}^{m} V_{bdiode,j}}{V_{omax}} \quad (1)$$

Where $V_{bswitch,\ i}$ and $V_{bdiode,\ j}$ refers to the maximum blocking voltage for switches and diode, respectively. V_{omax} is the peak value of output voltage.

Table 2. Switching stress for all switches

S_1	S_2	S_3	S_4	S_5	S_6
V_{in}	V_{in}	$2V_{in}$	$2V_{in}$	$2V_{in}$	$2V_{in}$

3. MODULATION STRATEGY

In multilevel inverters, various modulation strategies are used to generate a semi-sinusoidal output waveform. The multicarrier pulse width modulation technique is used in this paper to provide gate signals for the switches. As in [27] to generate an inverter switching signal, an N-level inverter requires (N-1) carrier waveforms that are compared to a reference signal. In this study, the four carriers are resulted from comparing a sinusoidal waveform as a reference with four carriers that are symmetrical in amplitude and frequency but different offset voltage, as shown in figure 3. It depicts the four carrier signals V_{cr1} to V_{cr4}. By comparing a reference signal with four carrier signals, it generates 4 pluses (X_1-X_4) and these pulses are transmitted to the 6 switches via the logic gate design displayed in figure 4. based on table [1]. The logic pattern is created from four pulses (X_1-X_4). (X_1) represents the output of comparison of (V_{ref}, V_{cr1}), (X_2) represents (V_{ref}, V_{cr2}), and so on, as well as the gate signals generated by the switching logic and the comparison, which are demonstrated in figure 5. The modulation index of the PWM is shown as follows:

$$MI = \frac{V_{ref}}{2V_{cr}} \quad (2)$$

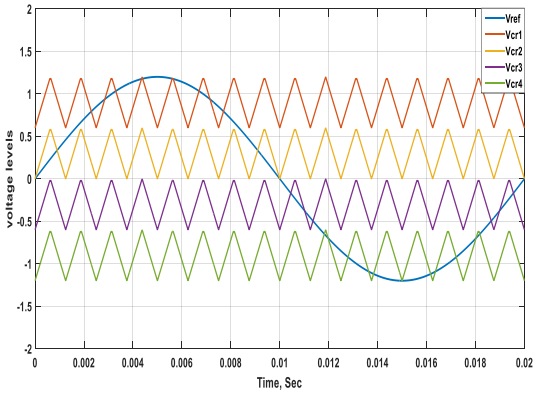


Figure 3. The modulation technique

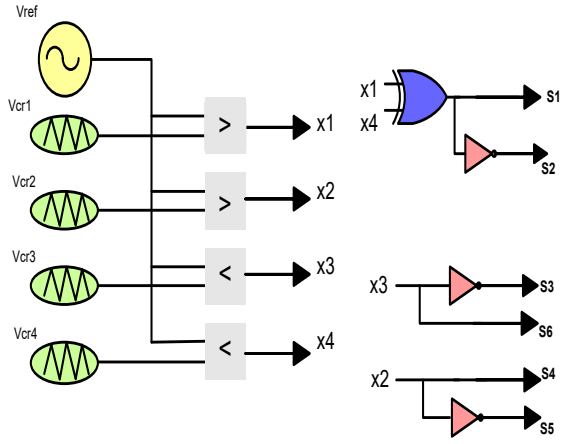


Figure 4. Logic pattern of gate signals

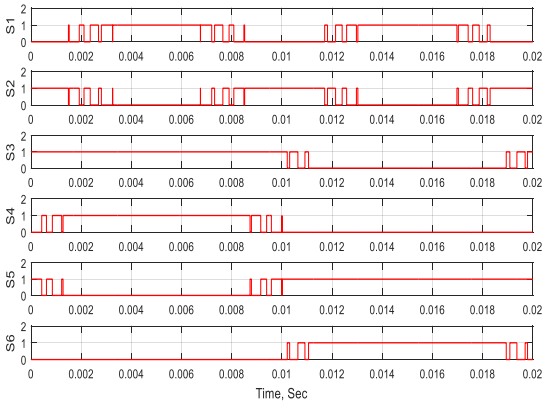


Figure 5. Gate pulses for six switches

4. CAPACITOR VOLTAGE BALANCING

One of the basic specifications of this architecture is that capacitor (C) is a self-balancing voltage. According to table 1, capacitor (C) is charged when the load voltage is zero & V_{in}. The capacitor' voltage (C) will be the same to the DC voltage if it considers that the voltage drops via switches and diodes are ignored. When the circuit is operating in the boost mode, i.e., when the inverter's load voltage is $2V_{in}$, the capacitor with the input source is discharged. So, a capacitor in SCDBMLI is self-balanced. There is no need for an additional control loop as the inverter's output voltage reaches the aimed value due to the parallel series paths when the circuit is in charging mode or discharging mode. Calculation of capacitor voltage is carried on using equation (3):

$$V_c = V_{in} \quad (3)$$

5. COMPARISON STUDY OF MULTILEVEL INVERTER

A comparison study is carried out on the suggested five-level configuration with different configurations to focus on the advantages of the suggested multilevel topology. The parameters of comparison is done for component counts, total voltage stress, the maximum number of (turn-on)switches at one mode, and gain as depicted in table [3]. The circuit necessitates six switches, which is less than the topologies in [16- 24]. The topology proposed in [22] does not provide a voltage gain despite using three capacitors and a greater number of switches. The $TSV_{p.u.}$ is a low value compared to topologies [16], [17], [19], [20], [21], [22], and [24]. Conduction losses were reduced as the switch count was reduced. However, in [23] and [24] the same boosting is achieved with three capacitors. As a result, the inverter cost is determined by the total stand voltage and the number of components per level. The inverter's cost is decreased if the TSV value is low, and vice versa [28-30]. To evaluate several configurations, a factor known as the cost function can be determined concerning the number of load voltage levels, as shown via equation (4):

$$CF = \left(N_{SW} + N_{driver} + N_D + N_{CAP} + \frac{\alpha(TSV)_{p.u.}}{Gain}\right) \quad (4)$$

Equation (4) is indicated that the cost factor calculation is based on the amount of IGBT switches, diodes, capacitors, and drivers. Gain is also used to evaluate the boosting capability. The factor (α) is a weight coefficient, and its value can be close to one [31-32]. Therefore, the major objective of this research is to minimize the cost of the suggested inverter when compared to different topologies and reduce component count while maintaining low TSV.

Table 3. Quantitative comparison of architecture in terms of other topologies

	[16]	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	PT
N_L	5	5	5	5	5	5	5	5	5	5
N_{SW}	9	8	8	8	7	7	7	6	6	6
N_D	-	-	2	-	10	2	-	2	1	1
N_C	3	3	1	1	2	3	3	3	3	1
$N_{max\ ON\ sw}$	5	5	4	4	4	3	4	3	3	3
$TSV_{P.U}$	6	5.5	5	8	9	6	6.5	4.5	6	5
GAIN	2	2	2	2	2	2	-	2	2	2

N_L= number of levels, N_D= number of diodes (not including antiparallel and series connected to an IGBT), N_{sw}= number of switches, N_c = Number of capacitors, $TSV_{p.u}$= Total stand voltage (in per unit), $N_{max\ ON\ sw}$ =maximum number (ON) switches, [PT] = Proposed topology.

6. LOSS AND EFFICIENCY CALCULATIONS

In semiconductor devices, two different main types of losses, namely switching losses and conduction losses, can happen. Switching losses resulted from delayed turn-on and turn-off operations. Conduction losses are turned on by semiconductor on-state resistance [33]. Another type of loss in the SC MLI that is due to internal resistance of the capacitor and semiconductor devices is capacitor loss [34].

6.1 Conduction losses

Semiconductor switches have a conduction loss when they are operated. Due to the switch's ON-state resistance and the voltage drop across the switch, losses happen when it is in the ON state. Switch and diode conduction losses, respectively, may be determined using equations (5) and (6):

$$P_{con\_sw} = V_{sw\_on} * i_{sw\_avg} + R_{sw\_on} * i^2_{sw\_rms} \quad (5)$$

$$P_{con\_D} = V_{D\_on} * i_{D\_avg} + R_{D\_on} * i^2_{D\_rms} \quad (6)$$

where P_{con_sw} denotes the conduction loss for each switch and P_{con_D} is the conduction loss for each diode. V_{sw_on} represents the ON-state voltage across the switch, V_{D_on} represents the on-state voltage across the diode, and R_{sw} on and R_D on represent the ON-state resistance of the switch and diode, respectively. i_{sw_avg}, i_{sw_rms}, i_{D_avg}, and i_{D_rms} are the switch and diode average and rms currents, respectively.

$$\begin{aligned}
P_{con(V_o=+1V_{dc})} &= 3\left(V_{sw_on} * i_{sw_avg} + R_{sw_on} * i^2_{sw_rms}\right) + (V_{D_on} * i_{D_avg} + R_{D_on} * i^2_{D_rms}) \\
P_{con(V_o=+2V_{dc})} &= 3\left(V_{sw_on} * i_{sw_avg} + R_{sw_on} * i^2_{sw_rms}\right) \\
P_{con(V_o=-1V_{dc})} &= 3\left(V_{sw_on} * i_{sw_avg} + R_{sw_on} * i^2_{sw_rms}\right) + (V_{D_on} * i_{D_avg} + R_{D_on} * i^2_{D_rms}) \\
P_{con(V_o=-2V_{dc})} &= 3\left(V_{sw_on} * i_{sw_avg} + R_{sw_on} * i^2_{sw_rms}\right)
\end{aligned} \quad (7)$$

The load voltage, the number of switches, and the diodes change in each stage during conduction. Therefore, using equation (7), the conduction losses are determined for each output level separately. Three switches and one diode are conducting at values of $+1V_{dc}$ and $-1V_{dc}$ respectively. Three switches alone are in the conduction at the $+2V_{dc}$ and $-2V_{dc}$ levels. By addition of the conduction losses at each level, as shown in Equation (8), the total losses during conduction are calculated.

$$P_{con(total)} = P_{con(V_o=+1V_{dc})} + P_{con(V_o=+2V_{dc})} P_{con(V_o=-1V_{dc})} + P_{con(V_o=-1V_{dc})} \quad (8)$$

6.2 Switching losses

Non-instantaneous turn-off and turn-on operations cause switching losses. When the switch is turned on, the collector current (I_C) starts increasing when the gate-emitter voltage (V_{GE}) rises beyond the threshold voltage (V_T). In addition, the collector-emitter voltage (V_{CE}) begins to decrease to $V_{sw\text{-}on}$, and an I_C is reached to $I_{sw\text{-}on}$ within a ton of time. Both I_C and V_{CE} have limited non-zero values during this ton, resulting in ON-time switching losses, as shown in Equation (9). Furthermore, both I_C and V_{CE} have restricted toff time values throughout the turn-off process, leading in the turn-off switching losses shown in Equation (10). Where $P_{SL,\ I\ (ON)}$ denotes the i_{th} switch's turn-on switching loss and $P_{SL,\ I\ (OFF)}$ denotes the i_{th} switch's turn-off switching loss.

$$P_{SL,i(on)} = f_{cr} \int_0^{t_{on}} V_{sw\_off,i(t)} * i(t)\, dt = f_{cr} \int_0^{t_{on}} \left(-\frac{V_{sw\_off,i}}{t_{on}} (t - t_{on}) \right) \left(\frac{I_{sw\_on,i}}{t_{on}} t \right) dt$$

$$= {}^1\!/_6 f_{cr} * V_{sw\_off,i} * I_{sw\_on,i} * t_{on} \quad (9)$$

$$P_{SL,i(off)} = f_{cr} \int_0^{t_{off}} V_{sw\_off,i(t)} * i(t)\, dt = f_{cr} \int_0^{t_{off}} \left(\frac{V_{sw\_off,i}}{t_{off}} t \right) \left(-\frac{I_{sw\_off,i}}{t_{off}} (t - t_{off}) \right) dt = {}^1\!/_6 f_{cr} * V_{sw\_off,i} * I_{sw\_on,i} * t_{off} \quad (10)$$

To calculate the overall switching losses of all switches, add the total turn-ON and turn-OFF losses of all switches using Equation (11).

$$P_{SL(total)} = \sum_{i=1}^{N_{sw}} \left(\sum_{j=1}^{N_{on(i)}} P_{SL,on(ij)} + \sum_{j=1}^{N_{off(i)}} P_{SL,i(off)} \right) \quad (11)$$

Where $P_{SL(Total)}$ is defined by the overall switching losses and N_{sw} is the overall number of switches and $Ns_{\_on}$ & N_{s_off} are the turn-ons and turn-offs count in single cycle, respectively, in the MLI topology.

6.3 Capacitor losses

Voltage drop across capacitance reactance and electric series resistance (ESR) cause capacitor losses. The capacitor is connected in parallel with the source during charging mode. The voltage differential (Vc) between the capacitor's actual and desired voltage causes ripple loss.

$$\Delta V_c = \frac{1}{c} \int_0^{t_c} I_c(t) \mathrm{d}t \quad (12)$$

$$E_{rl} = \frac{1}{2} C \Delta V_c^2 \quad (13)$$

The ripple loss (P_{rl}) can be deterimined using equations (12), (13), and (14). The higher value of P_{rl} can be reduced to low value by increasing capacitance. However, there must be a trade-OFF between sizing and capacitor ripple loss.

$$P_{rl} = f_o E_{rl} = \frac{f_o}{2c} \left(\int_0^{t_c} I_c(t) dt \right)^2 \quad (14)$$

The (ESR) causes conduction losses in capacitors during discharging mode. The capacitor and source connected in series. These losses are approximated as follows:

$$P_{esr} = i_c^2 * R_{c\_esr} \quad (15)$$

Where f_o is the fundamental frequency. The efficiency of proposed inverter is estimated from Equations (16) and (17):

$$efficiency\ \eta = \left(\frac{P_{input} - P_{losses}}{P_{input}} \right) * 100 \quad (16)$$

$$efficiency \eta = \left(\frac{V_{dc} * I_{dc} - P_{con(total)} - P_{SL(total)} - P_{rl}}{V_{dc} * I_{dc}} \right) \quad (17)$$

Where η is MLI efficiency, V_{dc} & I_{dc} are input voltage and input current respectively, and $P_{con(total)}$ and $P_{SL\ (total)}$ are total conduction and switching losses respectively of the total switches.

7. PERFORMANCE RESULTS AND DISCUSSIONS

This part presents both the experiment and simulation outcomes to validate the success of the suggested inverter. For various types of loads, simulation and experimental results were investigated. Table 4 lists the various parameters that were used to validate the topology which considers the same parameters in simulation and experimental. Simulation study for the suggested configuration is carried out using MATLAB/SIMULINK software. The inverter's load voltage, output current and harmonic spectrum are investigated. The section also includes a description of the laboratory's experimental setup. The Switching pulse system was implemented and tested using a digital signal processor (DSP) controller board (DS1104).

7.1 Simulation results

The performance for the configuration is examined under different conditions using (MATLAB-Simulink) at parameters listed in the table 4. Figure 6 depicts the signals of input voltage, inverter's load voltage, output current and capacitor voltage for RL-load with (f_{sw}) equals 100 Hz. It is evident that the voltage of output consists of five levels with a maximum value of 200 V for input voltage equals 100 V. The output current is sinusoidal and capacitor charges until its voltage is balanced at 100 V.

The voltage stress of all the switches at (f_{sw}) = 100Hz is shown in figure 7. The value shown in table [2] corresponds exactly to the voltage stress. The signals of input voltage, capacitor voltage, inverter's voltage and output current for RL-load at (f_{sw}) = 5000 Hz demonstrate in figure 8. It has been noted that increased switching losses are a result of more switching occurring at each level as a result of an increase in carrier frequency. Conversely, raising the carrier frequency causes the harmonics to shift to a higher order, which minimizes the size of the filter in grid-connecting applications. At (fsw) = 5000 Hz, figure 9 depicts the voltage stress on each switch.

Table 4. Parameters values for simulation and experimental

Circuit parameter	Simulation and Experimental
Input DC supply	100V
Switching frequency (f_{sw})	Hz 100,5000
R-load	Ω 100
RL-load	R=100 Ω, L=150 mH
capacitor	µF 990

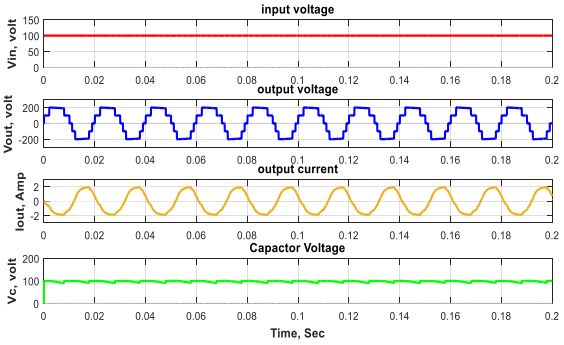


Figure 6. Input voltage, load voltage, output current, and capacitor's voltage for (R-L) Load at (f_{sw}) =100 Hz.

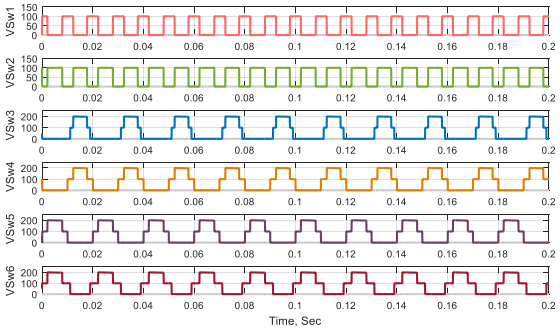


Figure 7. Voltage stress for (f_{sw}) =100Hz.

A case study is evaluated for load variations under three conditions which are (100 Ω), no-load, and (100Ω+150mH) at (f_{sw}) =100 Hz. The load voltage, load current, and capacitor's voltage are analyzed in figure 10. When a load is changed, the inverter's voltage is kept fixed while the output current varies. According to load type, the capacitor voltage is balanced and does not affect by load variation except in case of no load.

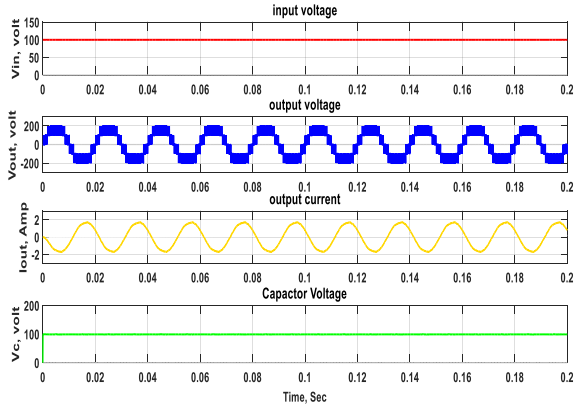


Figure 8. Input & inverter's voltage, output current, and capacitor voltage for (RL-load) for (f_{sw}) =5000Hz.

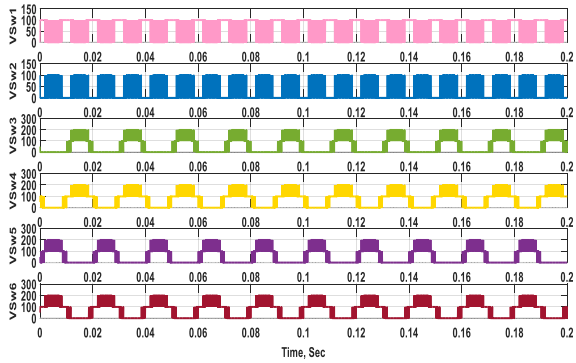


Figure 9. Voltage stress at (f_{sw}) =5000Hz.

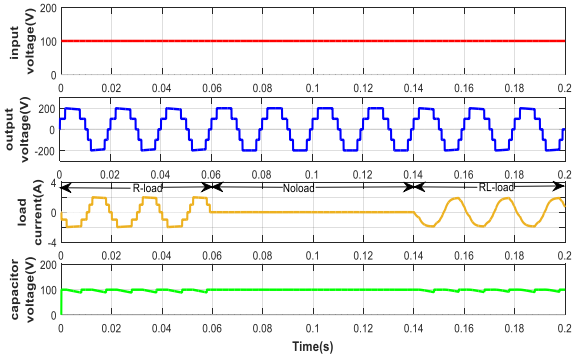


Figure 10. Input & inverter's voltage, output current, and capacitor's voltage for 100Ω, no load, and (100Ω+150mH), f_{sw}=100 Hz.

Another case study is taken for load variations from (100Ω+25mH) to (100Ω+150mH) in figure 11 at (f_{sw}) =100 Hz. The voltage and current of the inverter are shown, and as the inductive load increases, the output current decreases in magnitude and more lagging.

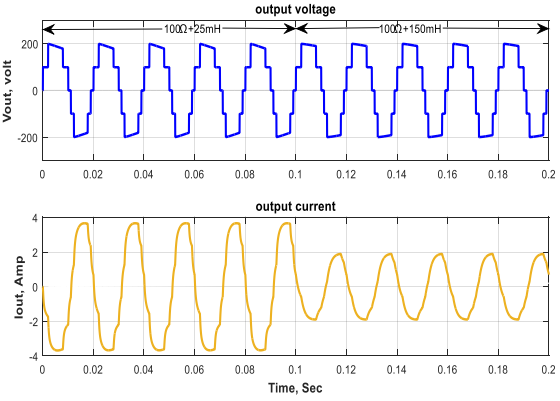


Figure 11. Load voltage and output current at RL-load =100Ω+25mH, 100Ω+150mH, (f_{sw}) =100 Hz.

The capacitor's voltage (c) demonstrates the self-balancing result of the capacitor at a change in the load condition. The change in input DC voltage is tested, which the DC voltage is different from 100 V to 200 V at (f_{sw}) = 5000 Hz. In figure 12, the inverter's voltage, load current, and capacitor's voltage are displayed. The capacitor's voltage is balanced from 100V to 200V and the inverter's voltage has five levels with a doubled boosting. Figure 13 illustrates the analysis of load voltage and output current at different Modulation Indexes (MI) of MI = 0.6, 0.8, and 1 at (f_{sw}) = 5000Hz. The voltage levels are maintained for these MI adjustments, but the $+2V_{dc}$ and $2V_{dc}$ level widths are changed.

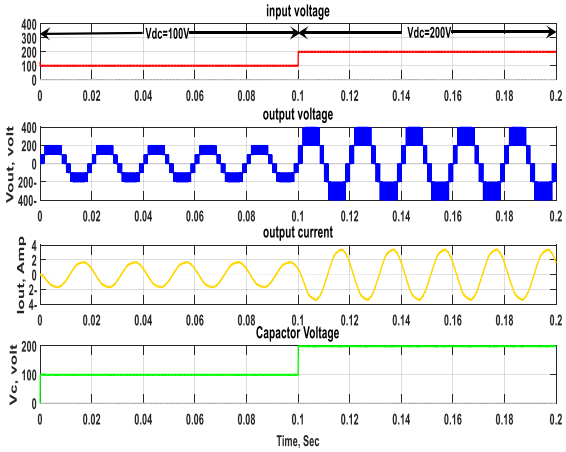


Figure 12. The input, load voltage, load current, and capacitor's voltage at the change of DC supply from 100V to 200V at (f_{sw})=5000Hz.

The Total Harmonic Distortion (THD) for output voltage at an input voltage of 100 volts, (f_{sw}) = 100 Hz is demonstrated in figure 14. The voltage THD in the case of R-load=100 Ω is 19.74%. The current THD waveforms when R-load=100 Ω is the same THD of voltage. Figure 15 shows current THD waveforms when RL- load=100Ω+150Mh at (f_{sw}) = 5000 Hz. .THD of the output current is around 3.45%

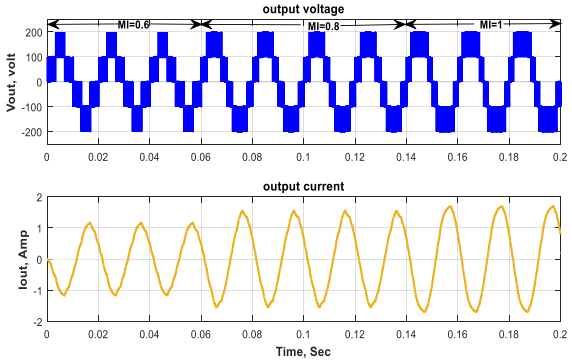


Figure 13. inverter's voltage and output current at MI = 0.6, 0.8, and 1 for load 100Ω+150mH, (f_{sw}) =5000 Hz.

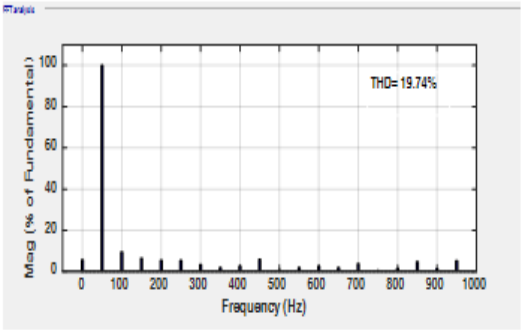


Figure 14. THD of the inverter's voltage at R-load

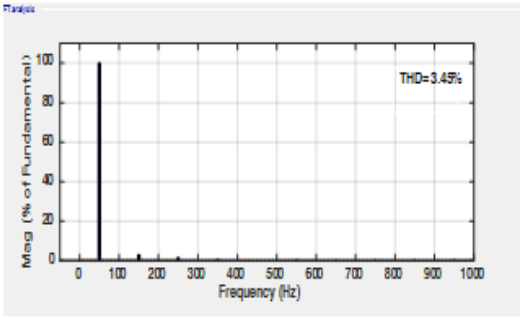


Figure 15. THD of inverter's current at RL-load

7.2 Experimental setup

The experimental configuration makes use of six IGBT switching devices. The inverter is built using IGBT modules of type (MITSUBISHI CM100DY-24H).

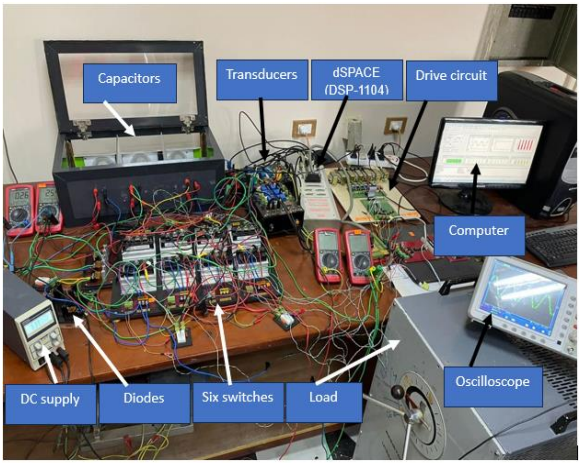
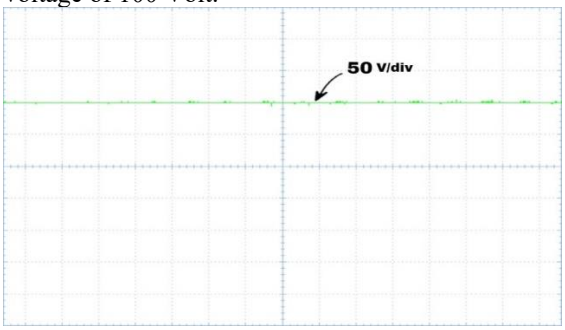


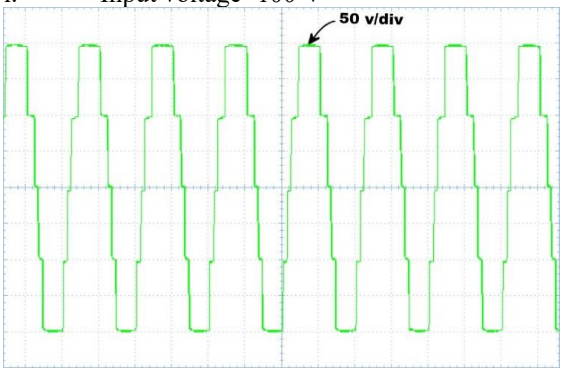
Figure 16. Experimental setup of the overall system

(dSPACE-1104) is used to implement the control system. Analog-to-digital converters transmit the sensors' (LA25-NP) output current measurements to the (dSPACE-1104) platform. Additionally, sensors are used to measure the output voltage and capacitor voltage. The drive pulse power obtained from (dSPACE - 1104) is amplified via an interface circuit to a higher level sufficient for controlling the inverter's gates and separating the control system from the power circuit. The experimental setup for the whole system is shown in Figure 16.

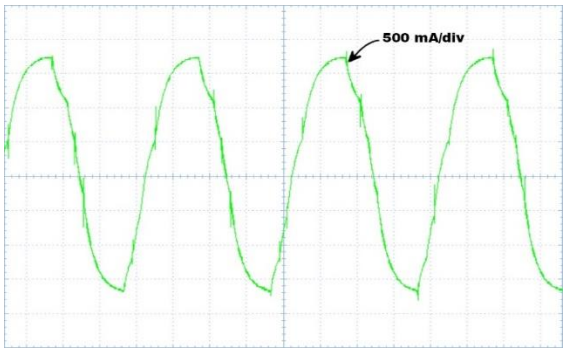
The oscilloscope demonstrates the input DC voltage is 100 V in figure 17 and the corresponding load, capacitor voltages, and output current at RL-load are shown at (f_{sw}) 100 Hz. In addition, the load current is shown for R-load to RL-load. However, the output voltage does not differ between (R, RL) loads. The capacitor voltage is self-balanced at V_C = 100 V without any need for a control circuit. The output voltage is 200 Volt which confirms twice the voltage gain. Figure 18 illustrates the similar results for (f_{sw}) 5000 Hz and the same input. The pulses of all switches are displayed in figure 19. It is detected that THD of the inverter's voltage and the output current for (f_{sw}) 5000 Hz within acceptable limits as shown in Figure .20 and figure 21, respectively. The overall efficiency would be around 97.6% in figure 22. Figure 23 depicts the voltage across switches S_1, S_4, and S_6 for input voltage of 100 Volt.



i. Input voltage=100 V



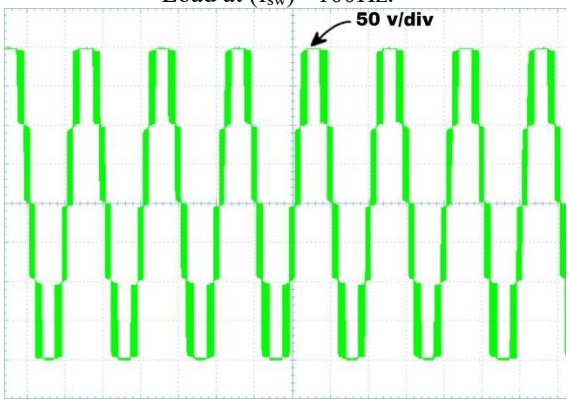
ii. load voltage at f_{sw} =100Hz



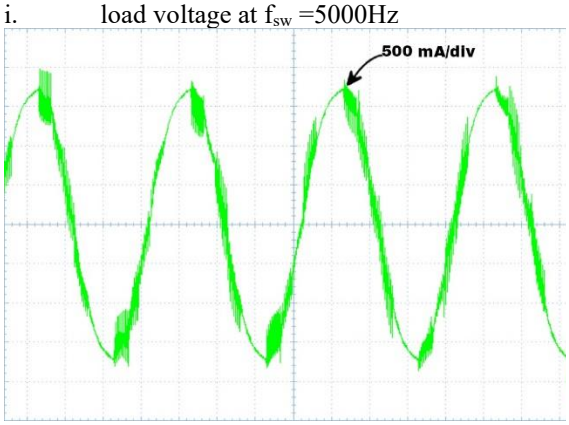
iii. load current at RL-load, f_{sw} =100Hz

iv. Capacitor voltage at f_{sw} =100Hz

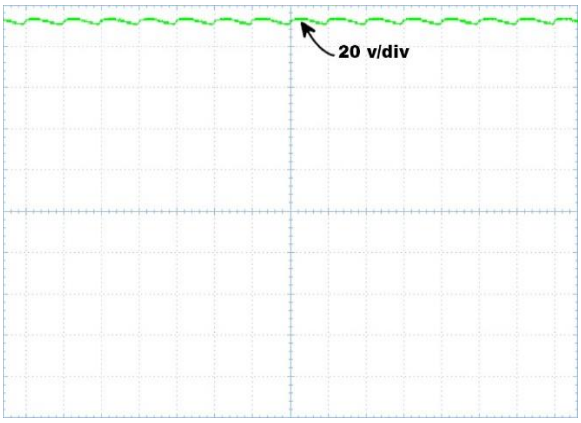
Figure 17. (i) Input voltage & (ii) load voltage, (iii) output current, and (iv) capacitor's voltage for RL-Load at (f_{sw}) =100Hz.



i. load voltage at f_{sw} =5000Hz



ii. load current of RL-load at f_{sw}=5000Hz



iii. Capacitor voltage at f_{sw} =5000Hz

Figure 18. (i) inverter's voltage, (ii) output current, and (iii) capacitor's voltage for RL-Load at (f_{sw}) =5000 Hz

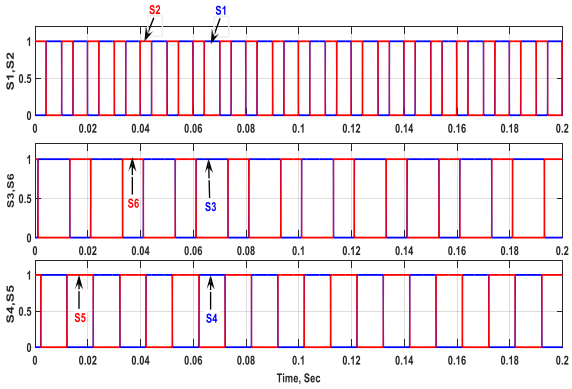


Figure 19. Pulses of all switches

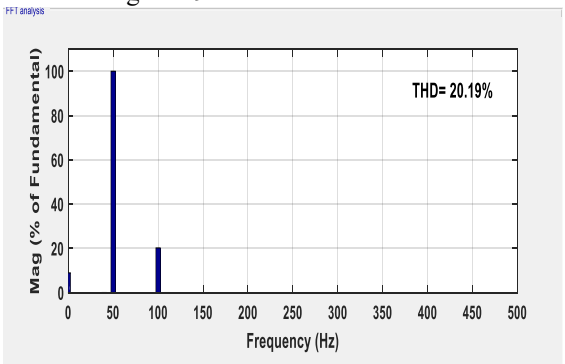


Figure 20. THD of output voltage for R-load

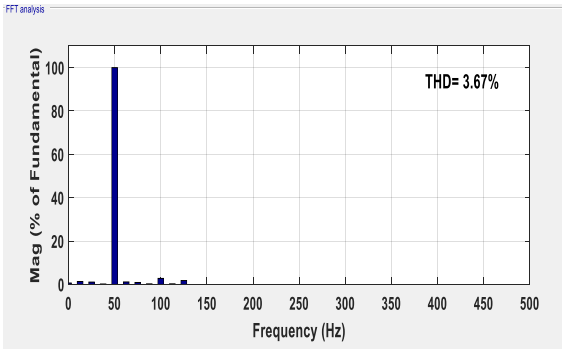


Figure 21. THD of output current for RL-load

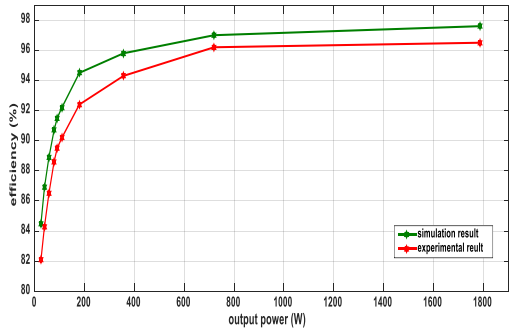
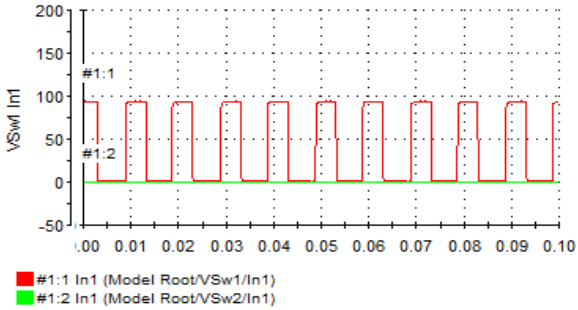
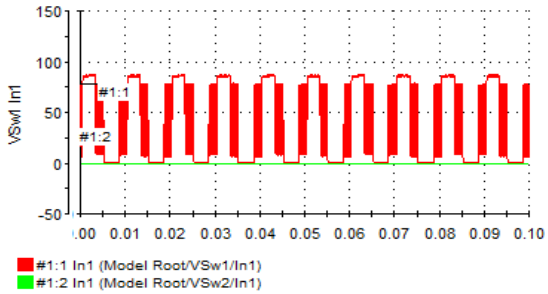


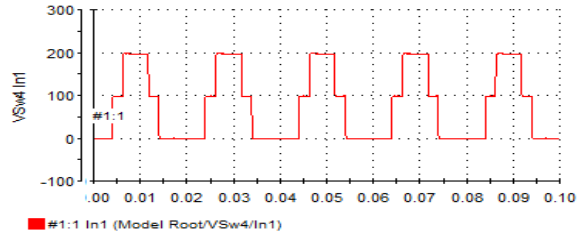
Figure 22. Efficiency in the 5-L output voltage



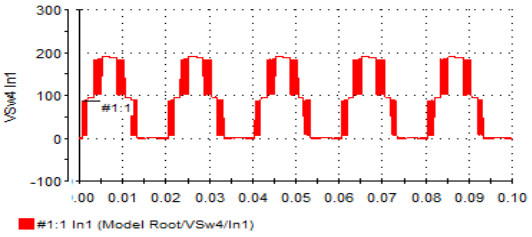
i. Voltage stress of S_1 at f_{sw} =100Hz



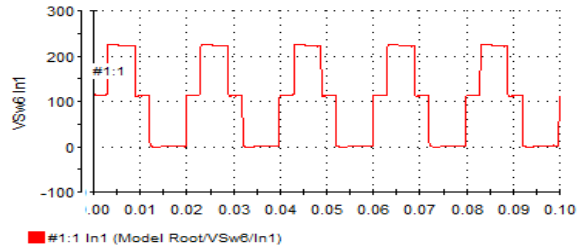
Voltage stress of S_1 at f_{sw} =5000Hz



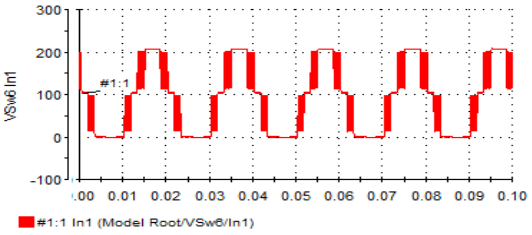
ii. Voltage stress of S_4 at f_{sw} =100Hz



Voltage stress of S_4 at f_{sw} =5000Hz



iii. Voltage stress of S_6 at f_{sw} =100Hz



Voltage stress of S_6 at f_{sw} =5000Hz

Figure 23. the experimental results, (i) voltage stress of S_1, (ii) voltage stress of S_4, (iii) voltage stress of S_6 at f_{sw} =100Hz & 5000Hz, respectively

5. CONCLUSIONS

The paper introduced a five-level MLI configuration. The suggested circuit is established on switched-capacitor technique with a lower number of switches, which includes six switches and one diode, as well as single capacitor with a single DC supply, to generate a five-levels at the output terminal with a double gain input supply and a reduced number of switches. Furthermore, it does not need any control system to balance voltage in the capacitor, reducing control complexity. A thorough comparison study demonstrates the proposed configuration has a reduced component for the same count of output levels. The suggested configuration's viability has been demonstrated by a variety of results under various loading conditions. The various simulation and experimental results validate the proposed configuration's improved performance.

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